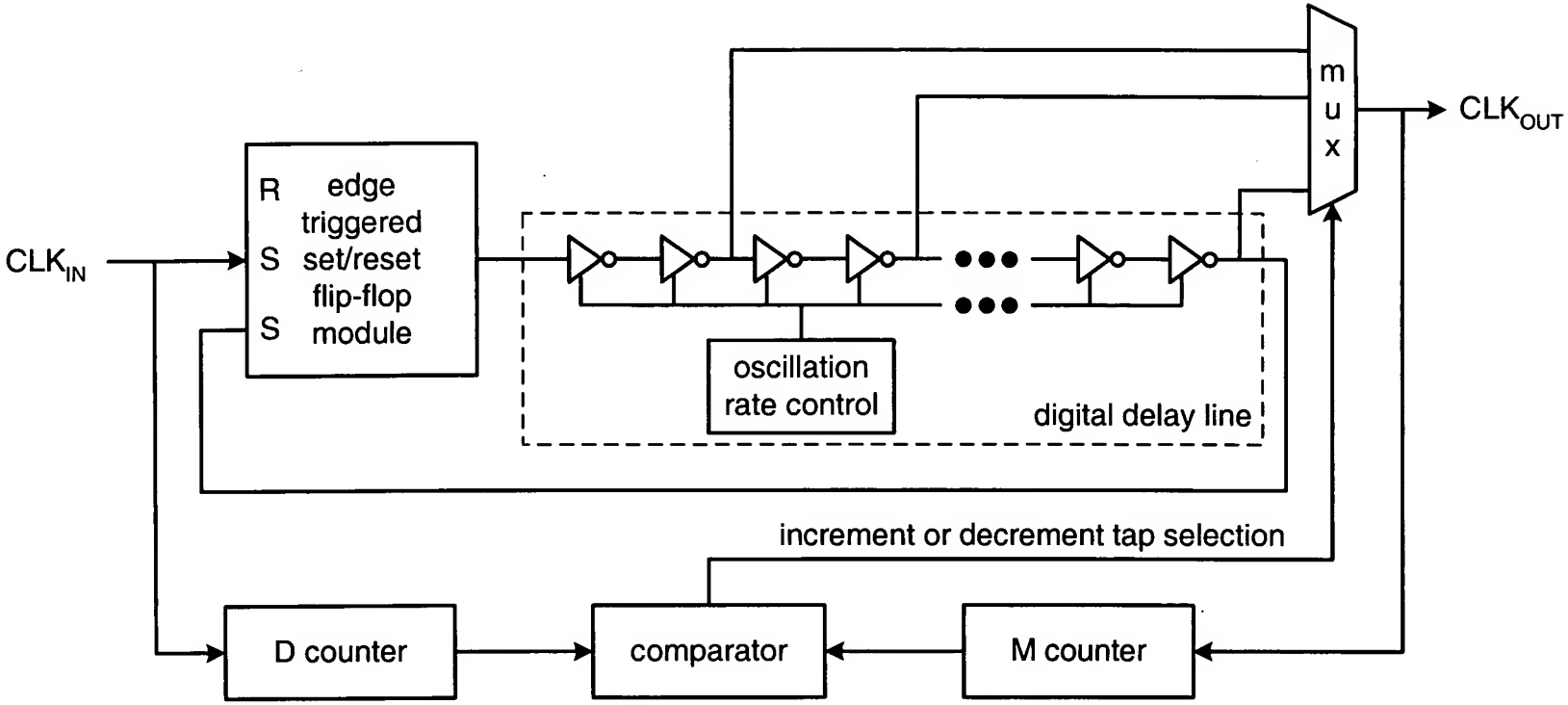


FIG. 1 - Prior Art

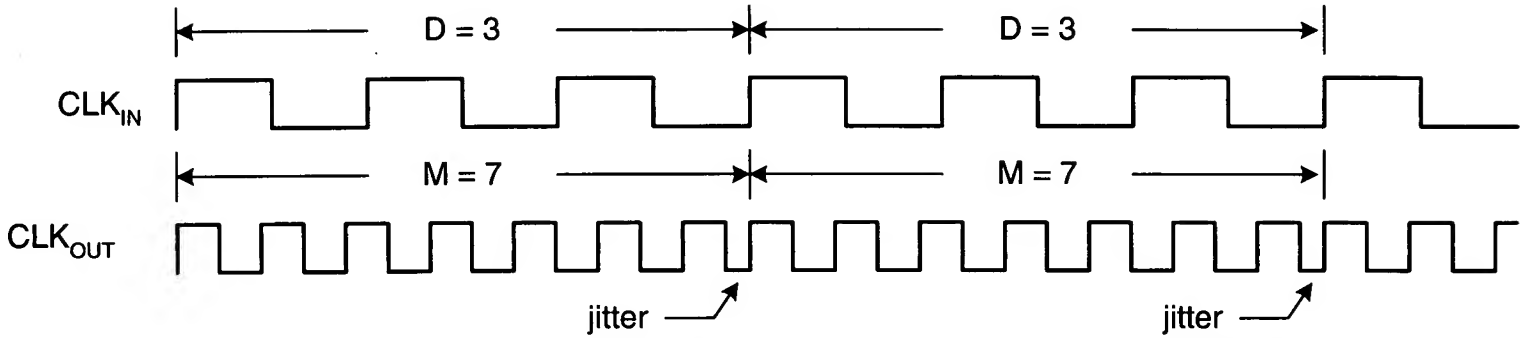


FIG. 2 - Prior Art $CLK_{OUT} = (M/D)*CLK_{IN}$

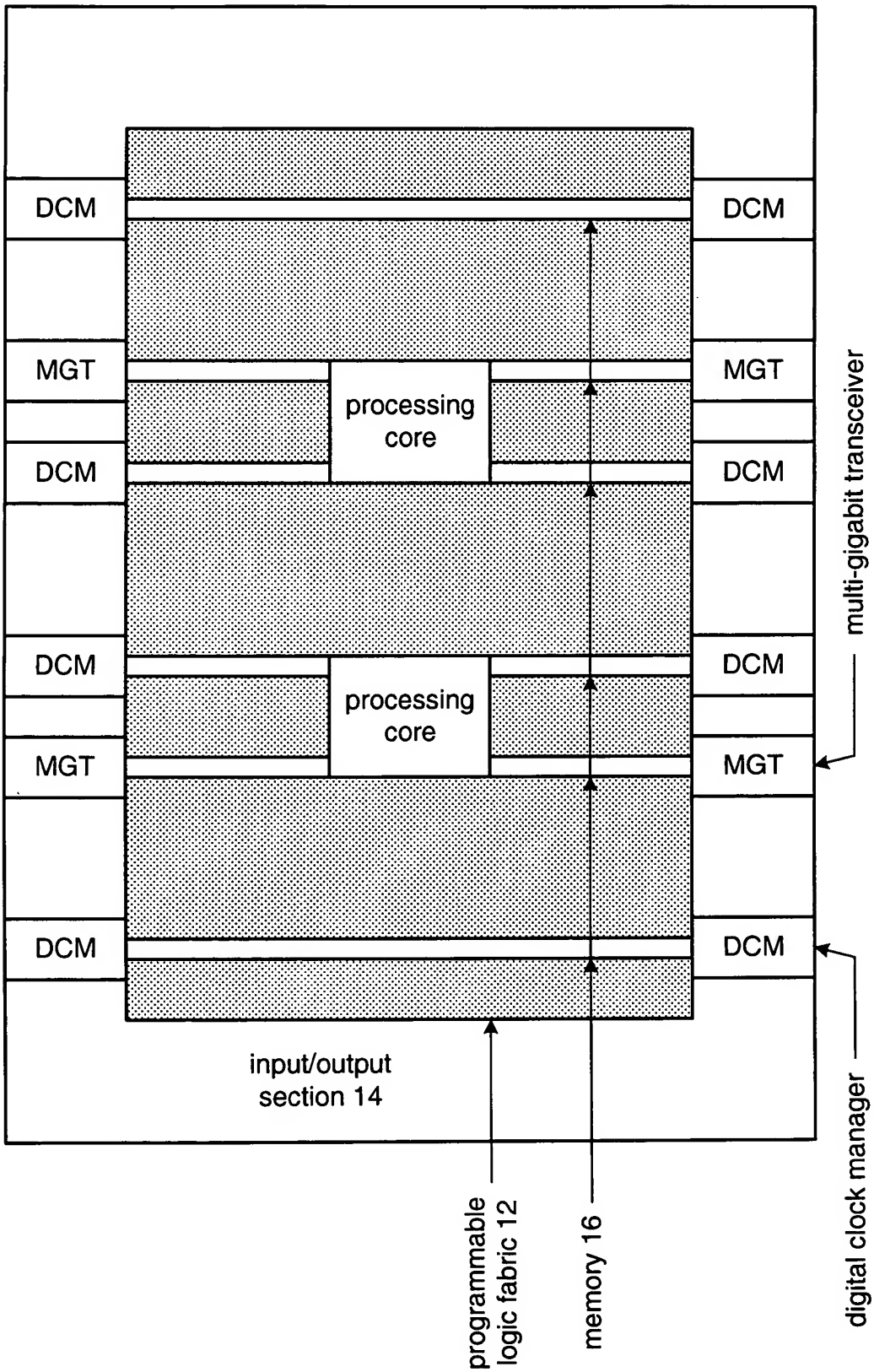

DCM
DCM
MGT
MGT
processing core
DCM
DCM
DCM
DCM
processing core
MGT
MGT
DCM
DCM
input/output section 14
programmable logic fabric 12
memory 16
digital clock manager
multi-gigabit transceiver
programmable logic device 10

FIG. 3

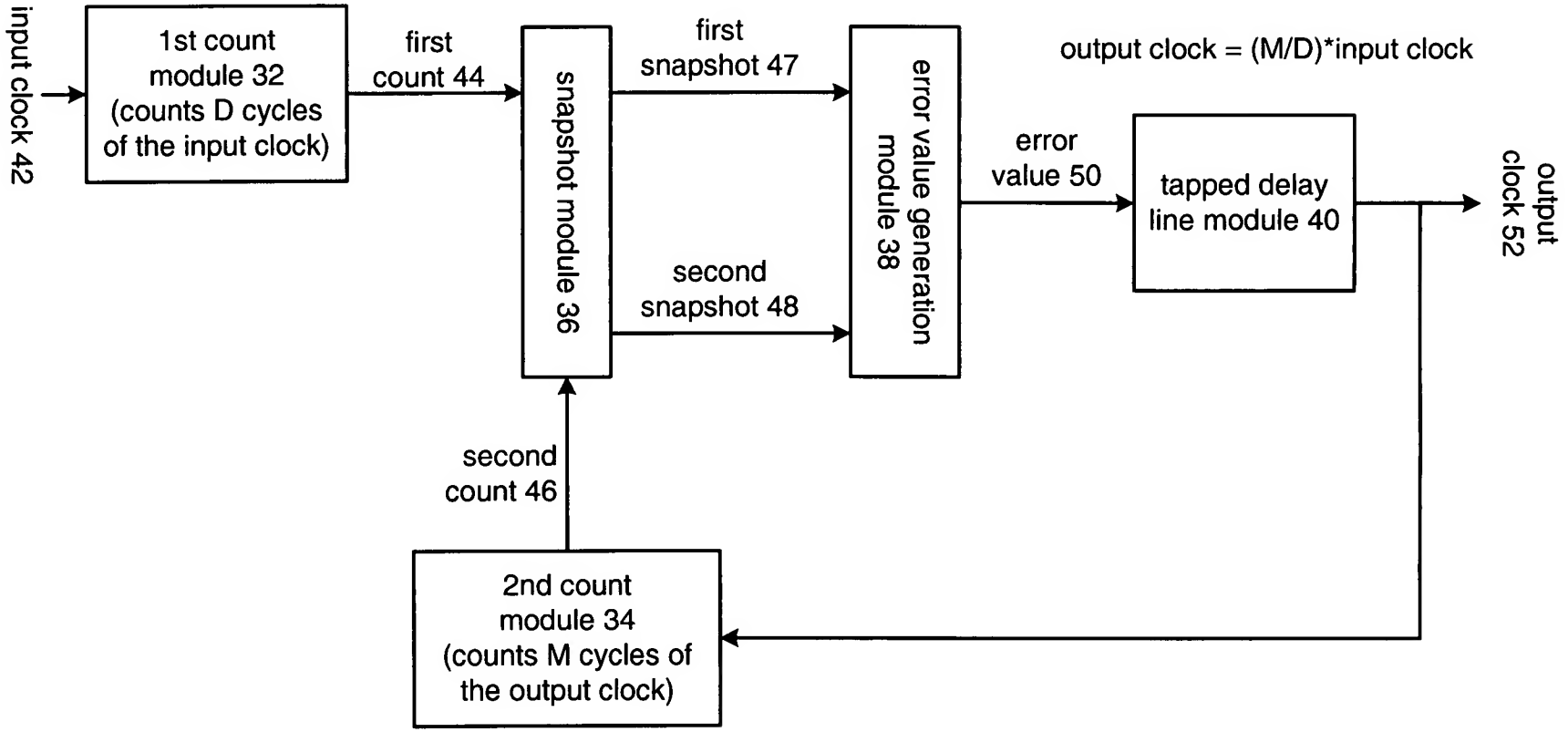


FIG. 4

DCM - low jitter digital frequency synthesizer 30

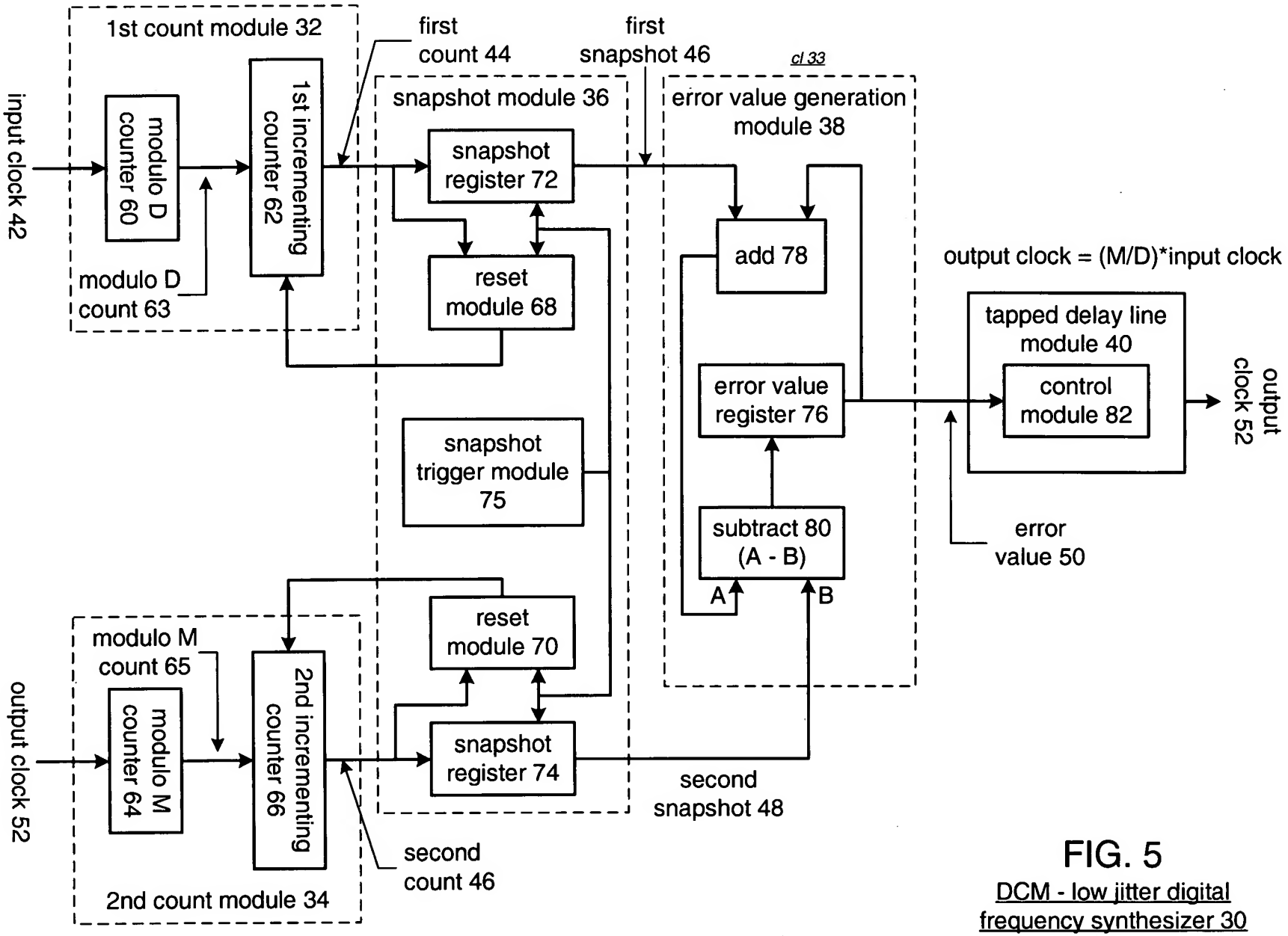


FIG. 5

DCM - low jitter digital frequency synthesizer 30

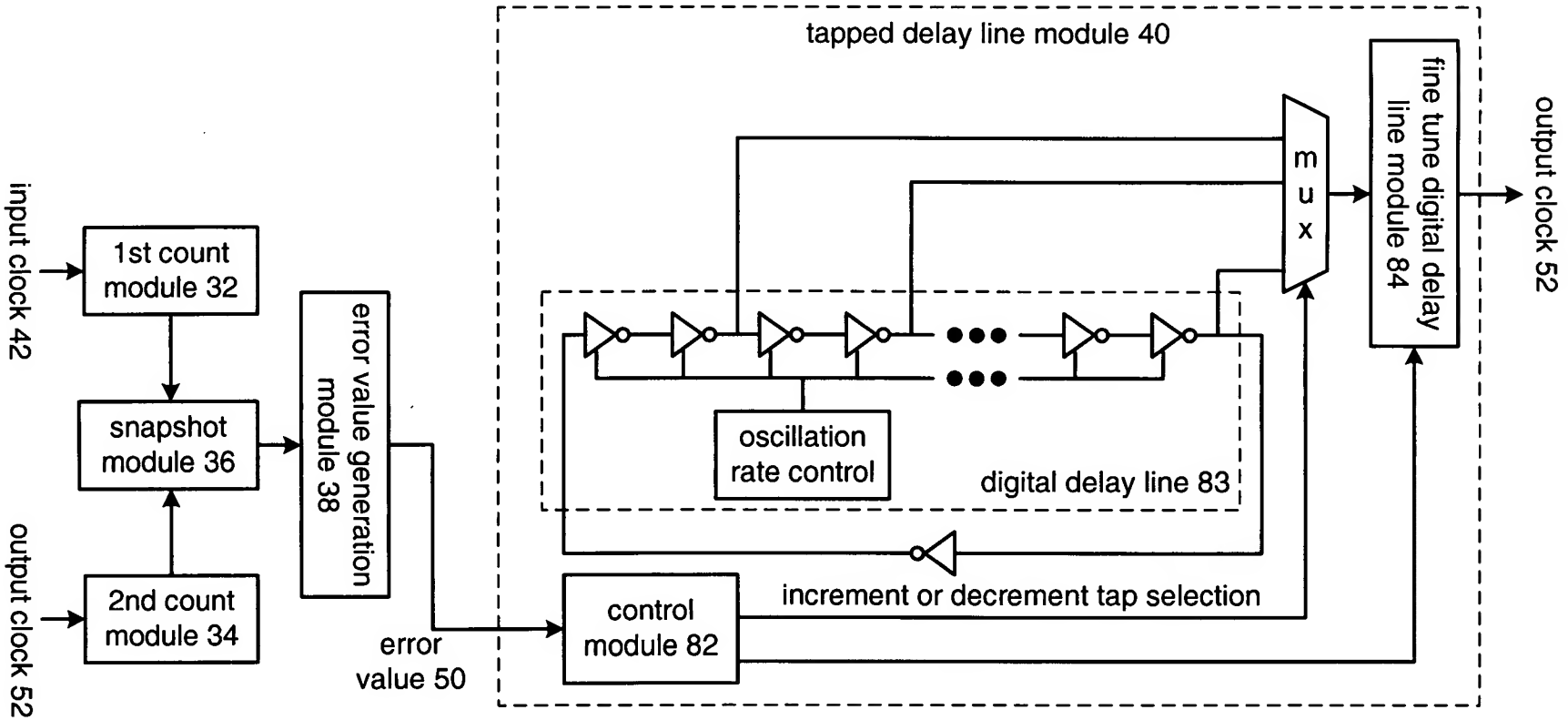


FIG. 6

$CLK_{OUT} = (M/D)*CLK_{IN}$

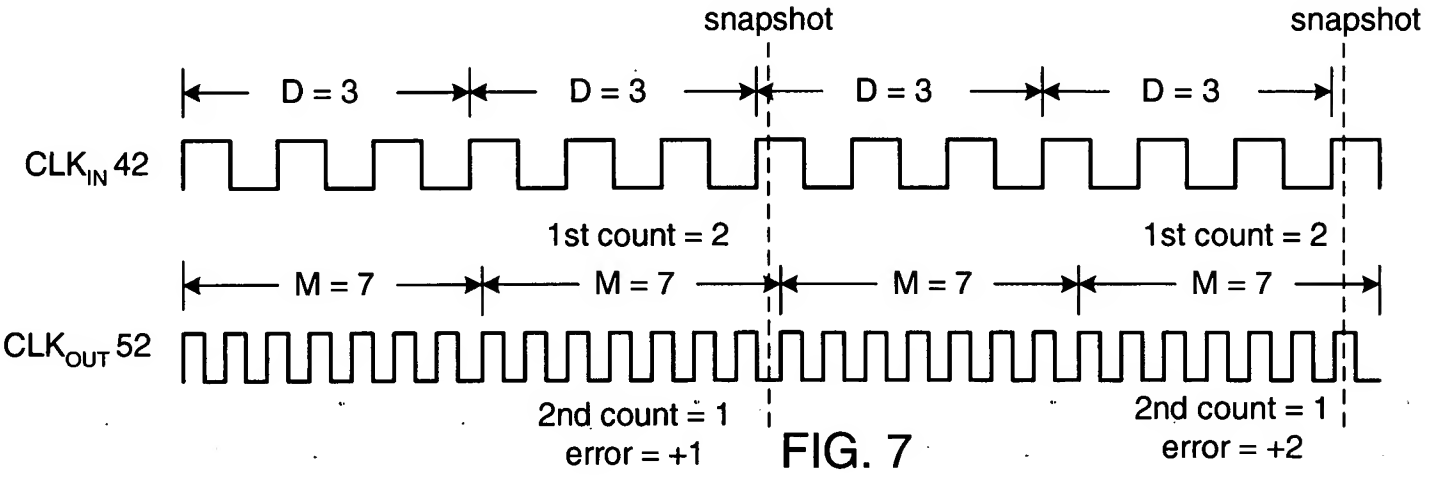


FIG. 7

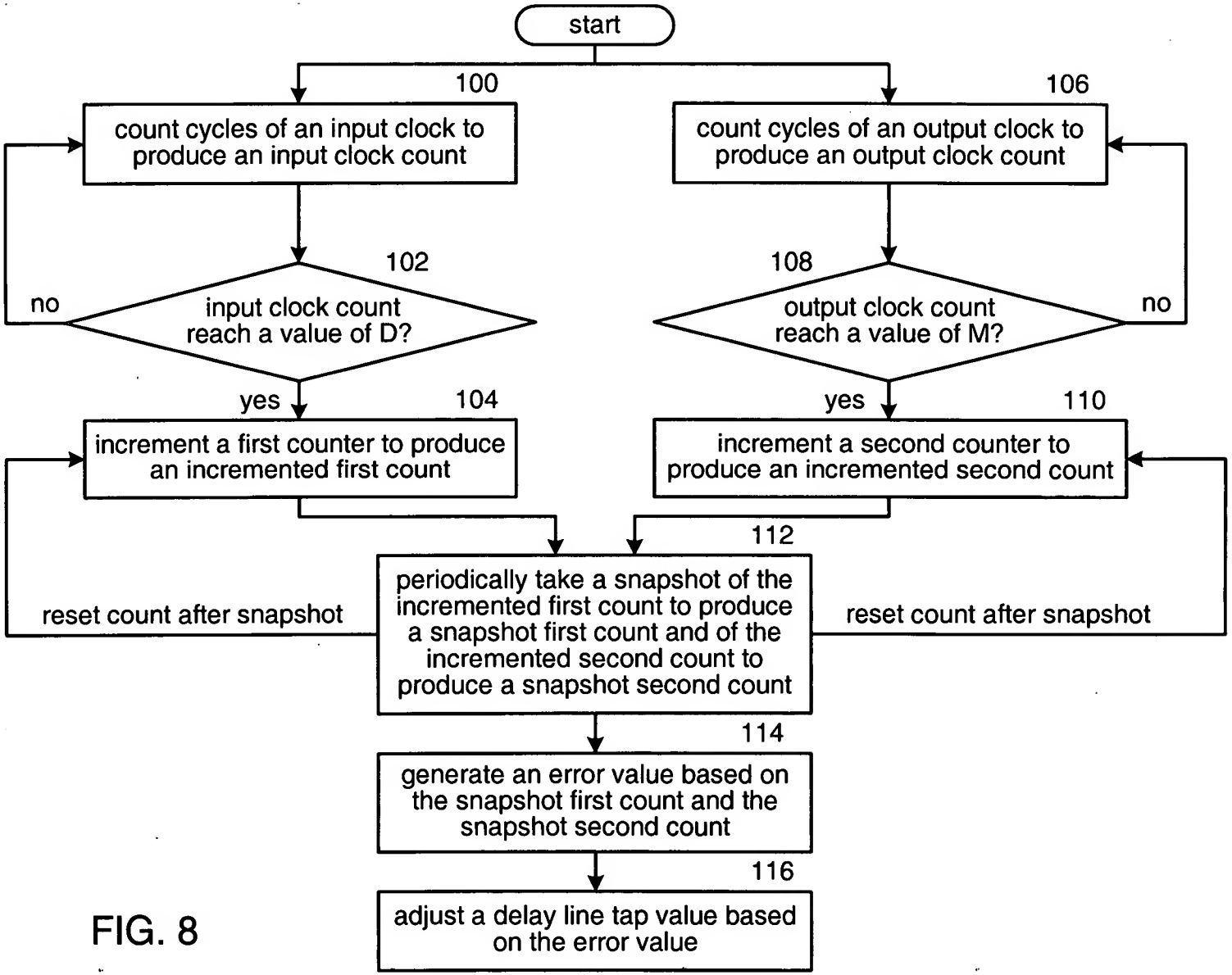

start
100
count cycles of an input clock to produce an input clock count
106
count cycles of an output clock to produce an output clock count
102
input clock count reach a value of D?
no
yes
108
output clock count reach a value of M?
no
yes
104
increment a first counter to produce an incremented first count
110
increment a second counter to produce an incremented second count
112
periodically take a snapshot of the incremented first count to produce a snapshot first count and of the incremented second count to produce a snapshot second count
reset count after snapshot
reset count after snapshot
114
generate an error value based on the snapshot first count and the snapshot second count
116
adjust a delay line tap value based on the error value

FIG. 8

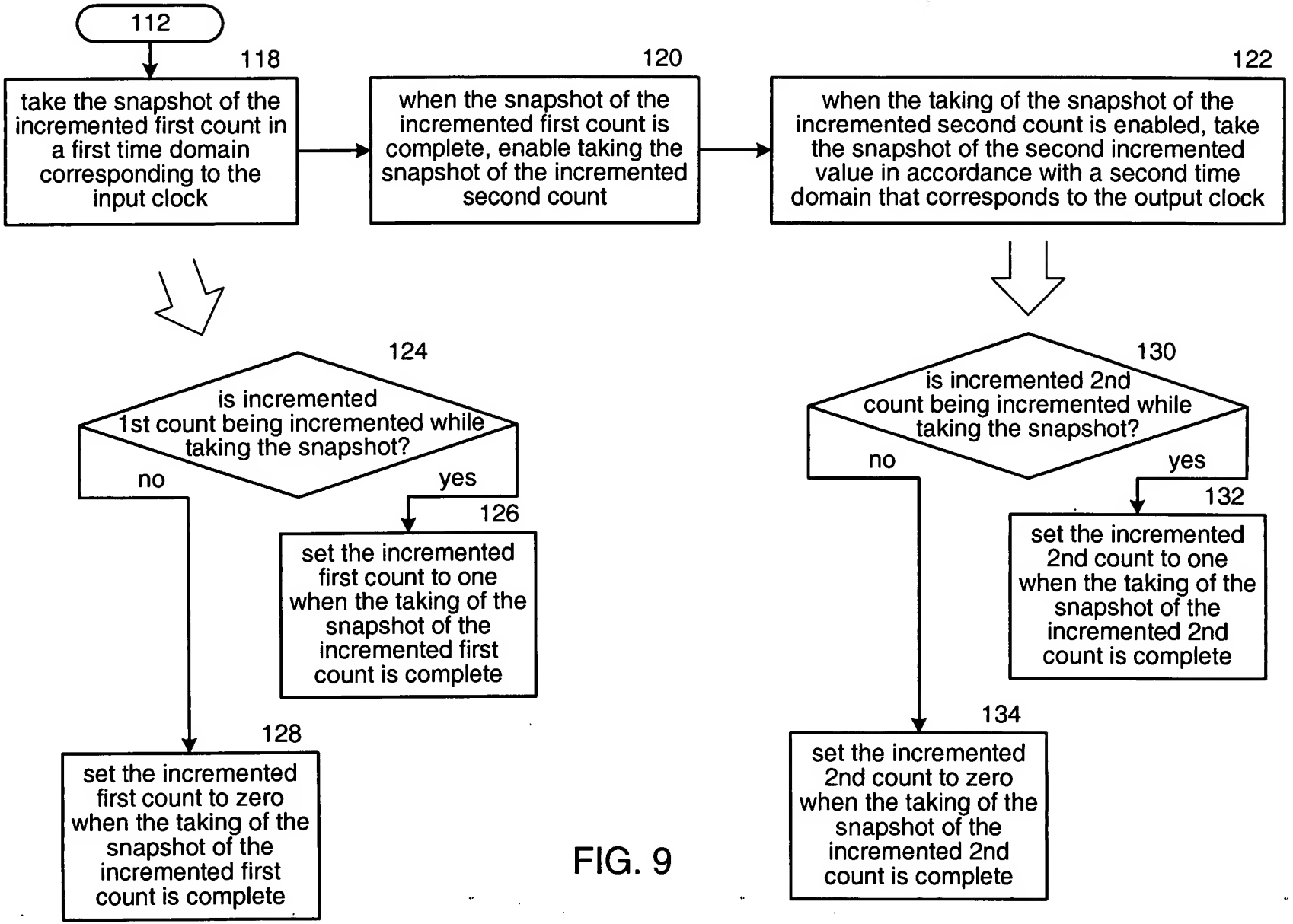

112
118
take the snapshot of the incremented first count in a first time domain corresponding to the input clock
120
when the snapshot of the incremented first count is complete, enable taking the snapshot of the incremented second count
122
when the taking of the snapshot of the incremented second count is enabled, take the snapshot of the second incremented value in accordance with a second time domain that corresponds to the output clock
124
is incremented 1st count being incremented while taking the snapshot?
no
yes
126
set the incremented first count to one when the taking of the snapshot of the incremented first count is complete
128
set the incremented first count to zero when the taking of the snapshot of the incremented first count is complete
130
is incremented 2nd count being incremented while taking the snapshot?
no
yes
132
set the incremented 2nd count to one when the taking of the snapshot of the incremented 2nd count is complete
134
set the incremented 2nd count to zero when the taking of the snapshot of the incremented 2nd count is complete

FIG. 9

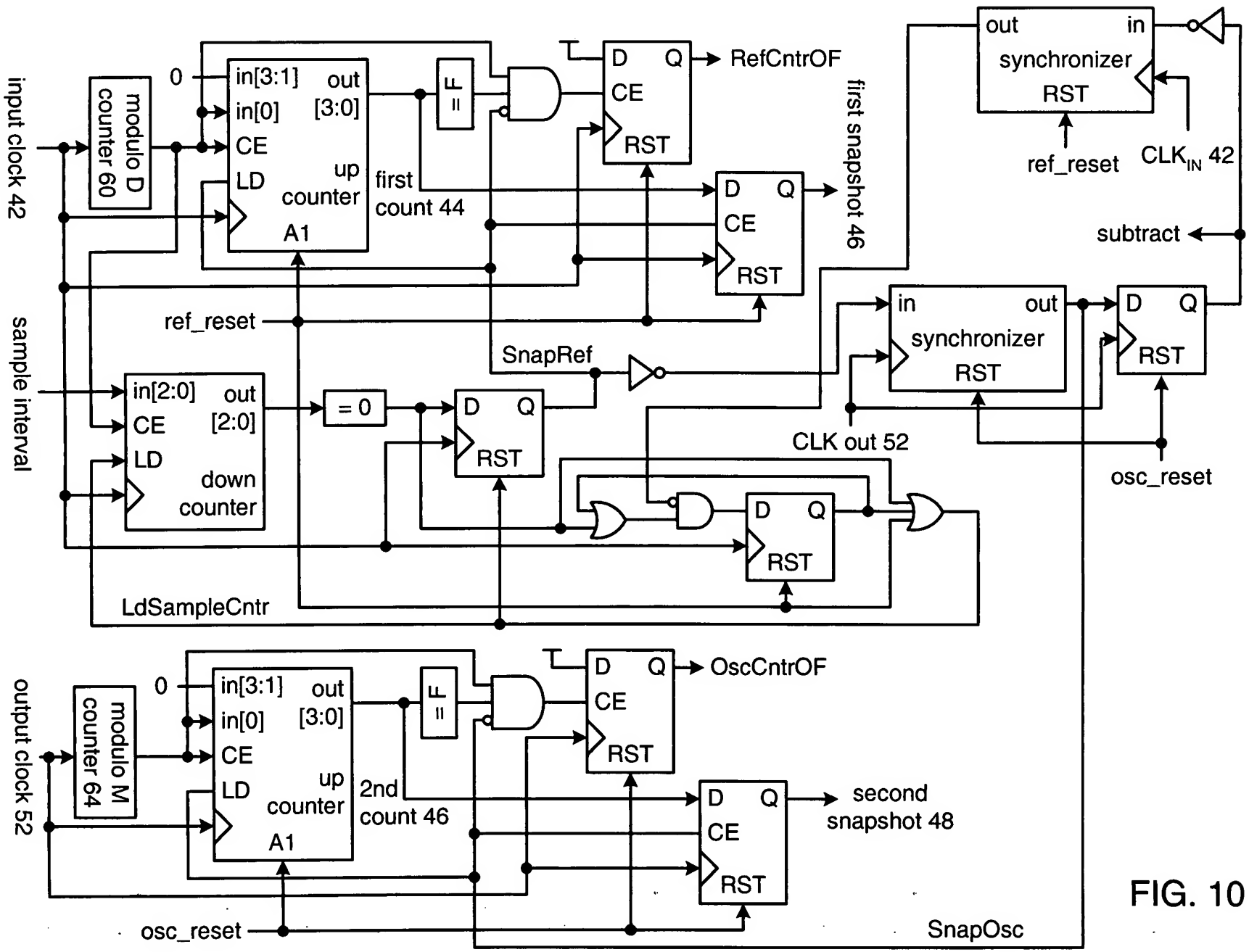

input clock 42
modulo D counter 60
0
in[3:1]
in[0]
CE
LD
out [3:0]
up counter
A1
first count 44
=
D
Q
CE
RST
RefCntrOF
first snapshot 46
out
in
synchronizer
RST
ref_reset
CLK$_{IN}$ 42
subtract
sample interval
in[2:0]
CE
LD
out [2:0]
down counter
= 0
SnapRef
CLK out 52
osc_reset
LdSampleCntr
output clock 52
modulo M counter 64
2nd count 46
OscCntrOF
second snapshot 48
SnapOsc

FIG. 10

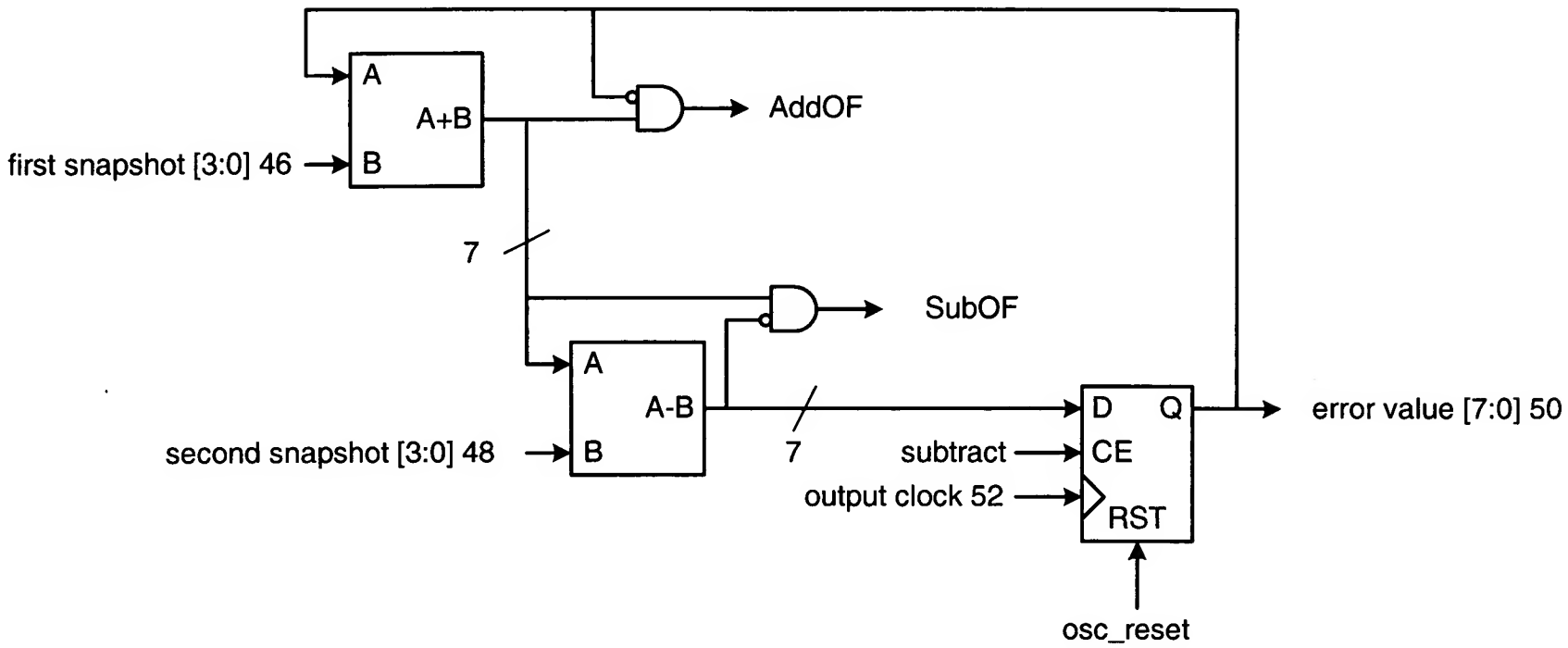


FIG. 11

error value generation module
38

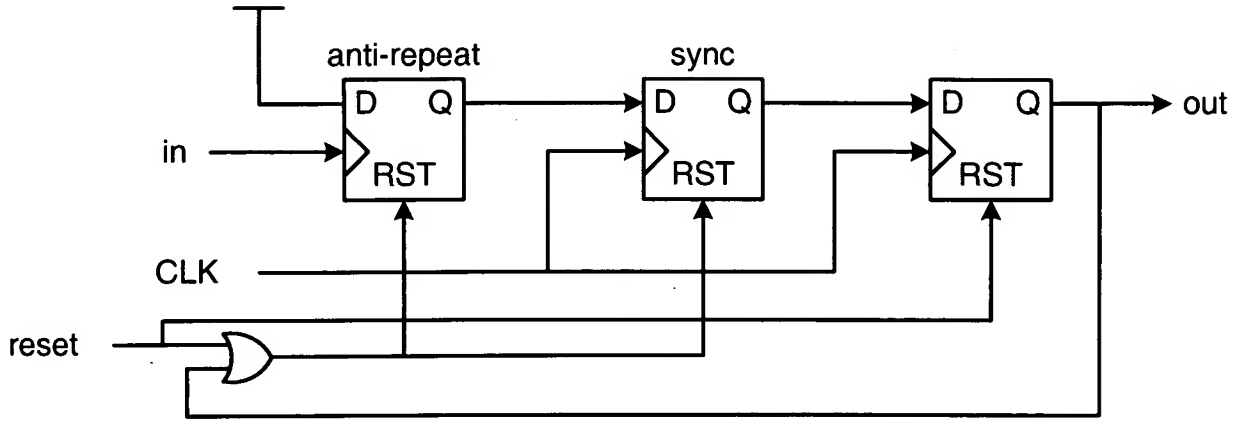


FIG. 12
synchronizer

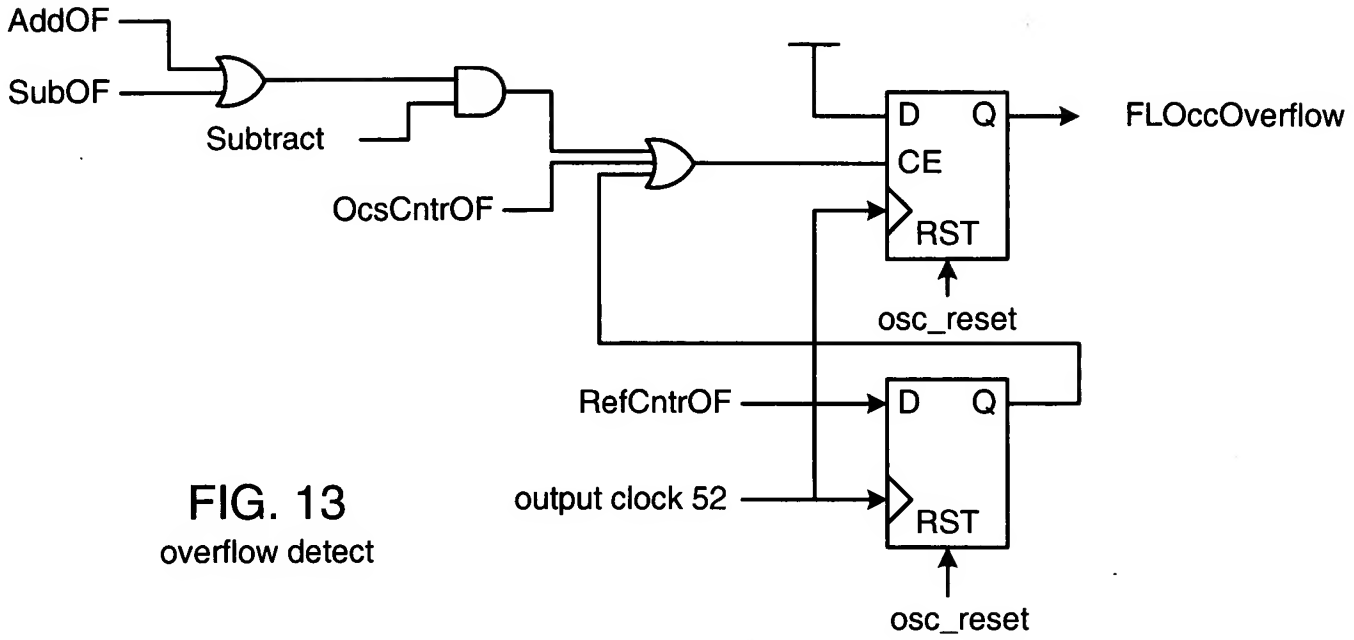


FIG. 13
overflow detect

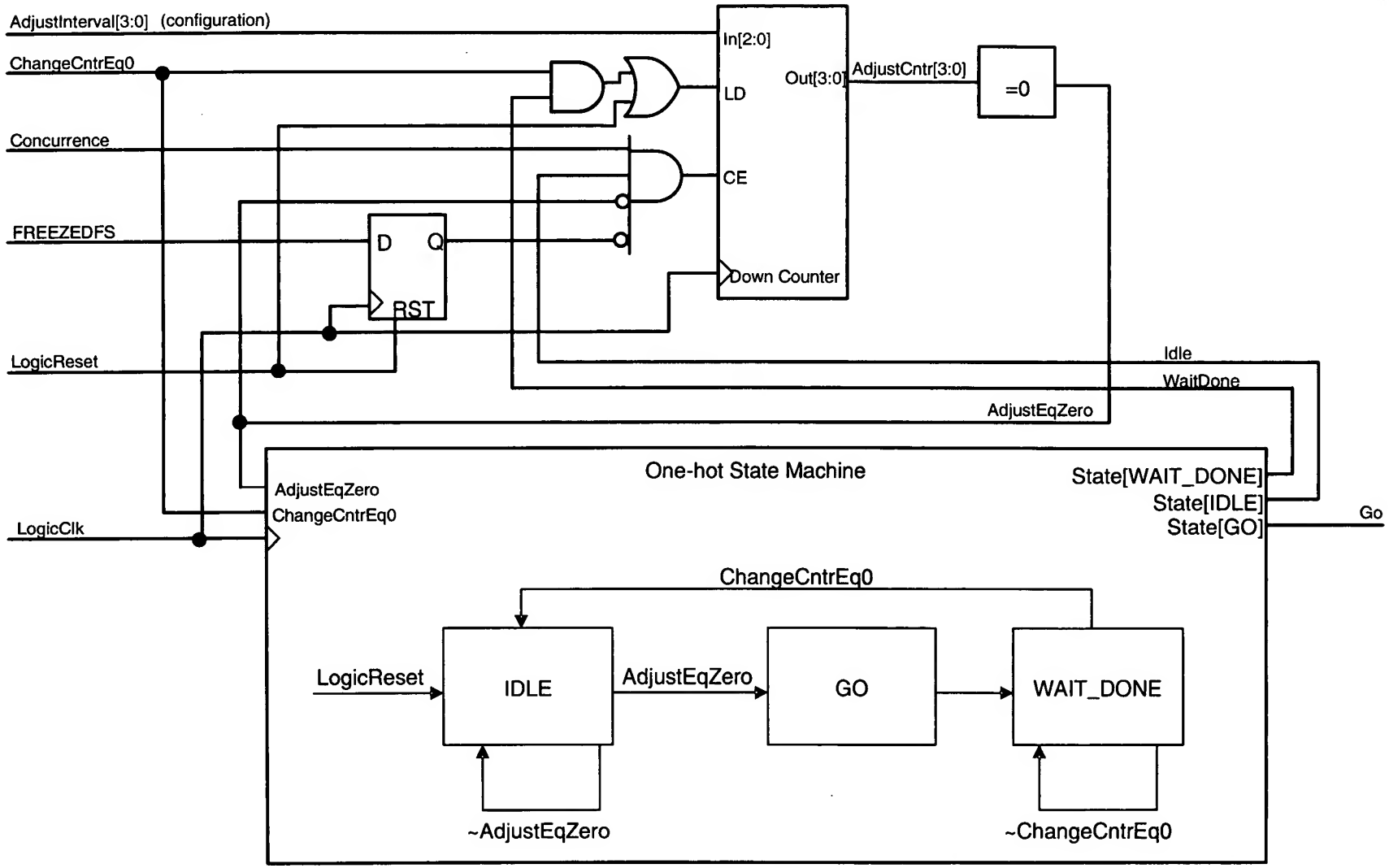
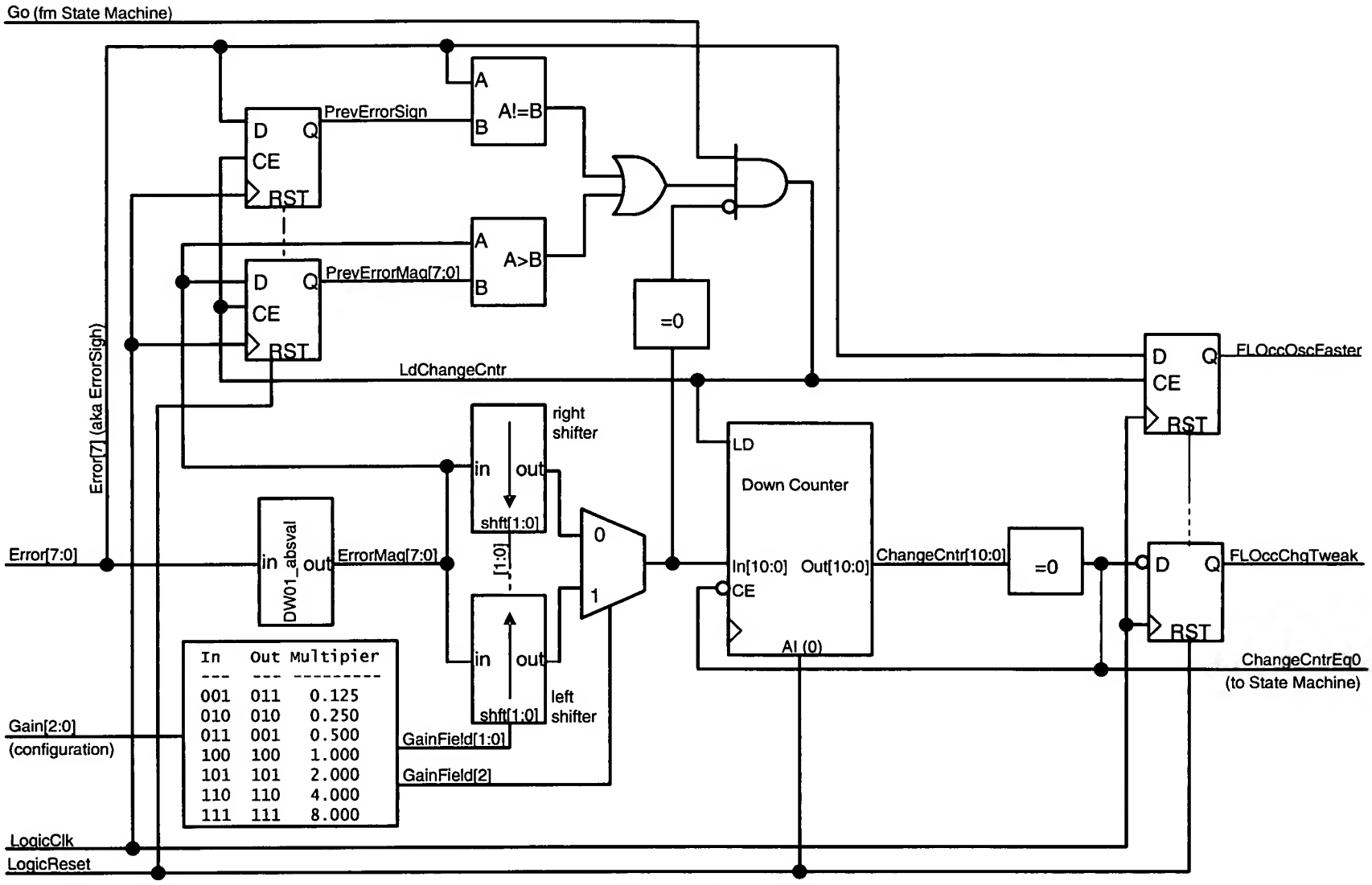


FIG. 14

tap/trim/ tweak adjust for tapped delay line 40



In	Out	Multipier
001	011	0.125
010	010	0.250
011	001	0.500
100	100	1.000
101	101	2.000
110	110	4.000
111	111	8.000

FIG. 15

tap/trim/ tweak adjust for tapped delay line 40